This listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A semiconductor IC structure comprising:

a semiconductor substrate; ~~including~~

a shallow trench isolation region located in said semiconductor substrate;

at least one front-end-of-the-line (FEOL) device ~~(FEOL)~~ located on a surface of said semiconductor substrate ~~thereof~~;

an etch stop layer located directly on said shallow trench isolation region;

~~at least one~~ a metal resistor ~~located on, or in close proximity to, said surface of said semiconductor substrate, said at least one metal resistor~~ comprising at least a conductive metal and located directly on and above said etch stop layer;

a dielectric material portion located directly on and above said metal resistor, wherein first sidewalls of said metal resistor and second sidewalls of said dielectric material portion are vertically coincident and said first sidewalls are directly adjoined to and located directly above said second sidewalls; and

a first level of metallization located above said ~~at least one~~ metal resistor.

Claim 2 (Cancelled)

Claim 3 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 4 (Original) The semiconductor IC structure of Claim 3 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

Claim 5 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 6 (Cancelled)

Claim 7 (Currently Amended) The semiconductor IC structure of Claim [[6]]1 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

Claim 8 (Cancelled)

Claim 9 (Original) The semiconductor IC structure of Claim 1 wherein said first level of metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

Claim 10 (Original) The semiconductor IC structure of Claim 1 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claims 11 – 40 (Cancelled)

Claim 41 (New) The semiconductor IC structure of Claim 1 wherein a periphery of a first cross-sectional area enclosed by said first sidewalls of said metal resistor and a periphery of a second horizontal cross-sectional area enclosed by said second sidewalls of said dielectric material portion are congruent.

Claim 42 (New) A semiconductor IC structure comprising:

a semiconductor substrate;

a planarized dielectric material portion having a substantially planar horizontal top surface and located on said semiconductor substrate;

at least one front-end-of-the-line (FEOL) device located on a surface of said semiconductor substrate and beneath said planarized dielectric material portion;

a metal resistor comprising at least a conductive metal and located directly on and above said planarized dielectric material portion;

a dielectric material portion located directly on and above said metal resistor, wherein first sidewalls of said metal resistor and second sidewalls of said dielectric material portion are vertically coincident and said first sidewalls are directly adjoined to and located directly above said second sidewalls; and

a first level of metallization located above said metal resistor.

Claim 43 (New) The semiconductor IC structure of Claim 42 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 44 (New) The semiconductor IC structure of Claim 42 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 45 (New) The semiconductor IC structure of Claim 42 wherein said first level of metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

Claim 46 (New) The semiconductor IC structure of Claim 42 wherein a periphery of a first cross-sectional area enclosed by said first sidewalls of said metal resistor and a periphery of a second horizontal cross-sectional area enclosed by said second sidewalls of said dielectric material portion are congruent.

Claim 47 (New) A semiconductor IC structure comprising:

a semiconductor substrate;

a shallow trench isolation region located in said semiconductor substrate;

at least one front-end-of-the-line (FEOL) device located on a surface of said semiconductor substrate;

a metal resistor comprising at least a conductive metal and located directly on and above said shallow trench isolation region;

a dielectric material portion located directly on and above said metal resistor, wherein first sidewalls of said metal resistor and second sidewalls of said dielectric material portion are vertically coincident and said first sidewalls are directly adjoined to and located directly above said second sidewalls; and

a first level of metallization located above said metal resistor.

Claim 48 (New) The semiconductor IC structure of Claim 47 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 49 (New) The semiconductor IC structure of Claim 47 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 50 (New) The semiconductor IC structure of Claim 47 wherein said first level of metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

Claim 51 (New) The semiconductor IC structure of Claim 47 wherein a periphery of a first cross-sectional area enclosed by said first sidewalls of said metal resistor and a periphery of a second horizontal cross-sectional area enclosed by said second sidewalls of said dielectric material portion are congruent.